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High-grade long-life electrolytic capacitors: the 106/107 series in power supply design

D. Mason

Mullard Industrial Electronics Division

The history of 'wet' electrolytic capacitors is outlined, and the successive structural, manufacturing, performance, quality, and reliability improvements that have been achieved, particularly in the Mullard 106/107 *range, are discussed.*

INTRODUCTION

There has been a generally held but out-of-date idea that electrolytic capacitors are unreliable and unpredictable, both in shelf life and in service. This concept needs to be revised. Given that a particular range of capacitor is properly manufactured, by up to date techniques, then correct selection from within that range can ensure long life. Manufacturers and users alike, who have investigated reasons for failure, will agree that over half of all capacitor failures are caused by incorrect selection.

This article gives a general background on capacitors, but in particular an insight into the manufacture and quality checking of the 106/107 range. Through this it shows their suitability for use in the modern circuit environment. The 106/107 range is illustrated graphically in Fig. 1.

MEETING THE NEEDS

Not only is there a very large call for power supply units designed and made as separate pieces of equipment, but virtually every equipment designed needs power supplied within it. These power supplies need smoothing and sometimes storage facilities. Equipments in general, and particularly computers, are experiencing a continuing process of increase in complexity. Thus the power supplies associated with them have consequently increased demands put on them for reliability, output current, and minimised physical size.

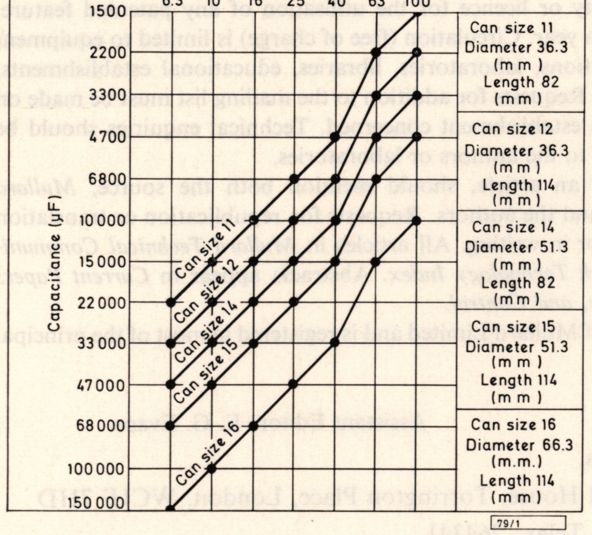

Fig. 1—Capacitance, working voltage, and can sizes of 106/107 series

The 106/107 range of high-capacitance electrolytics offers the user a high-grade, long-life component to meet those needs. It can handle approximately three times the ripple current of its predecessor, and it offers up to one farad.volt capacitance-voltage product, very low effective series resistance, and a working temperature range extended to 85°C. The mechanical properties are also significantly improved; the capacitors will stand up to severe bump and vibration conditions.

During the last decade considerable research and development has been carried out on all types of electrolytics, including high capacitance 'wet' electrolytics*. Continuous programmes of development normally produce gradual improvements in products. The Mullard development programme has of course been providing such continuous improvement, but the introduction of the new range of high-capacitance, high-grade wet electrolytics marks a significant step forward in this field. They are ideal for use in the power supplies of digital equipment, energy storage in pulse systems, and filters in measuring and control apparatus. Their long service life and high reliability make them suitable for both industrial and military applications.

CAPACITOR BACKGROUND

Electrolytic capacitors have an outstanding advantage in their high capacitance-to-volume ratio; a fact which makes their use in certain circumstances essential and in many other cases highly desirable. It is some ninety years since the electrolytic principle was noticed and some seventy years since, in Germany, the first electrolytic capacitor was made. Development has continued since then.

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*The term 'wet electrolytics' can be misleading if taken out of context, since in the past these were actually in the form of a self-contained bath of electrolyte with a central anode and often with the can as the cathode connection. Modern types are not of this construction. The types termed 'dry' should not however be confused with solid types, as in the Mullard 121 series solid electrolyte aluminium capacitors where a sintered solid semiconducting electrolyte is employed.

Capacitors of the 106/107 series

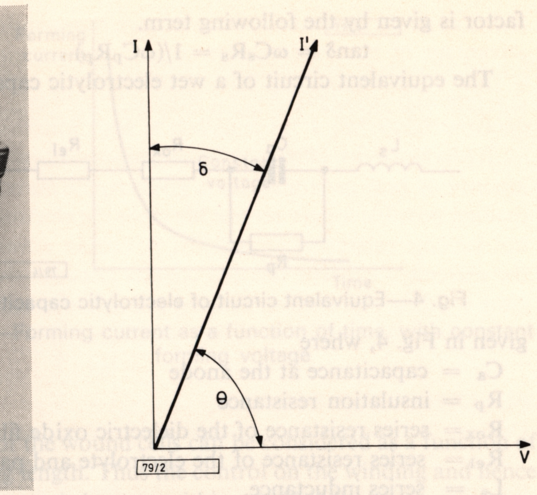

Fig. 2—Dielectric loss represented vectorially

All bodies possess some capacity for storing charge but, in the majority of cases, this charge leaks away through the imperfect insulation of the surrounding medium. Thus the storage capacity of most bodies is very small. A capacitor, however, is designed to have good charge storing properties.

The Leyden jar, which was a glass jar with metal foil on the inside and out, formed one of the earliest practical capacitors, and until about 1935 the Services used the 'jar' as a unit of capacitance*.

In the 1930s and for some time after this, wet electrolytic capacitors (often called aqueous electrolytic condensers) had a reservoir of liquid electrolyte contained in a can. The anode was often a central spiral strip or ribbed rod and the can was used as the 'cathode' connection to the electrolyte. In modern techniques the anode and 'cathode' are wound together, with the electrolyte absorbed in a spacer between the two.

The SI unit of capacitance is the farad (F). A capacitor is said to have a capacitance of one farad if a potential difference of one volt is developed when a charge of one coulomb is stored in the capacitor. Although it is generally accepted that the farad is much too large a unit for practical purposes, it becomes more of a reality now with the advent of the 106/107 series of capacitors. In calculation and circuit work, especially if electrolytic capacitors are being considered, the μF is used for convenience.

Two plates of metal, the electrodes, separated by air, form the simplest type of capacitor, air being the insulator or dielectric. Essentially a dielectric is a material in which the application of electric field gives rise to no net flow of electric charge, only a displacement of charge. It is this property that is exploited in capacitors, since the fact implies that dielectrics are capable of storing charge. When a charge is stored on one electrode an equal and opposite charge is induced on the other, and a potential difference is thus set up between the electrodes. For a given dielectric the charge storing property of the capacitor (its capacitance), is greater for larger electrode areas and for smaller electrode separation, and also depends on the nature of the dielectric. The following relationship gives the capacitance of a parallel plate capacitor:

$$C = kA/4\pi t$$

where

k = the permittivity of the dielectric
A = the surface area of the electrodes
t = the thickness of the dielectric film.

If a theoretical or ideal capacitor is placed across an alternating voltage, the current leads the voltage by a phase angle of 90°, that is $\pi/2$ or one quarter cycle. This means that there is zero loss in the capacitor since no power is being absorbed by the dielectric. In a practical capacitor this ideal situation does not, of course, apply since the dielectric will always give rise to some loss, however small. This is indicated vectorially in Fig. 2. The loss may occur because of migration of charge through the dielectric—known in practical terms as leakage current; dielectric absorption, which means that the charging or discharging current does not die away exponentially with time but continues for a much longer time as an appreciable value; or the ohmic resistance of the leads, electrodes, and associated connections.

This loss can be considered as occurring in a series or parallel resistance, as shown in Fig. 3. Thus the dissipation

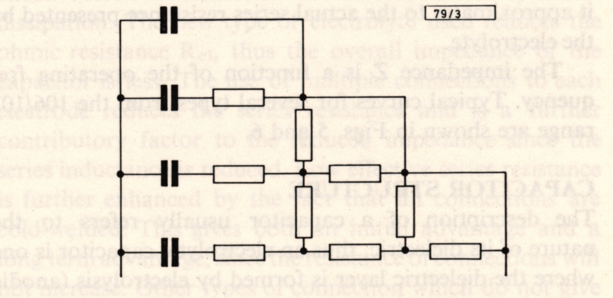

Fig. 3—Approximate equivalent circuit of capacitive interface

factor is given by the following term.

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*1μF equalled 900 jar. See Admiralty Handbook of Wireless Telegraphy, 1938, Vol. 1, sect. 168.

$$\tan\delta = \omega C_s R_s = 1/(\omega C_p R_p)$$

The equivalent circuit of a wet electrolytic capacitor is

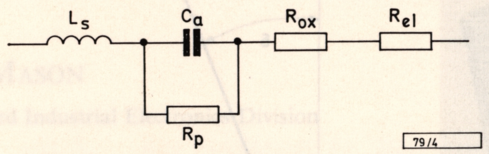


Fig. 4—Equivalent circuit of electrolytic capacitor

given in Fig. 4, where

C_a = capacitance at the anode
R_p = insulation resistance
R_{ox} = series resistance of the dielectric oxide film
R_{el} = series resistance of the electrolyte and paper
L_s = series inductance.

The dominant elements of the effective series resistance are R_{ox} and R_{el}. The leads, electrodes and connections also present resistance, but often this is a small percentage of the effective series resistance. This is certainly the case in the 106/7 series, since multiple cold-welded connections are made with low resistance material.

Since Fig. 4 is a representation of a practical capacitor, the designer is principally interested in the following measurements:

1) The capacitance C_a measured at 50Hz.
2) The loss factor, $\tan\ \delta = \omega R_s C_a$, measured at 50Hz, where $R_s = R_{ox} + R_{el}$
3) The impedance Z.

With large electrolytic capacitors used in power supplies, where normally ripple currents are low frequency, the significance of (1) and (2) is obvious. However, these capacitors are also used in applications covering a wide frequency range, and impedance is often of prime importance. From the equivalent circuit the impedance is as follows:

$$Z = \sqrt{\left[R_s^2 + \left(\frac{1}{j\omega C_a} - j\omega L_s\right)^2\right]}$$

The following approximations can be used at various frequencies:

$$\begin{array}{ll} 50\text{Hz} & Z \simeq \dfrac{1}{\omega C_a} \\ 100\text{kHz} & Z \simeq R_{el} \\ 10\text{MHz} & Z \simeq \omega L_s \end{array}$$

The above expressions show that, over a given frequency range, the impedance has a minimum value mainly dictated by the electrolyte. The impedance measured at a frequency of 100kHz is regarded as one of principal importance since it approximates to the actual series resistance presented by the electrolyte.

The impedance Z is a function of the operating frequency. Typical curves for several types from the 106/107 range are shown in Figs. 5 and 6.

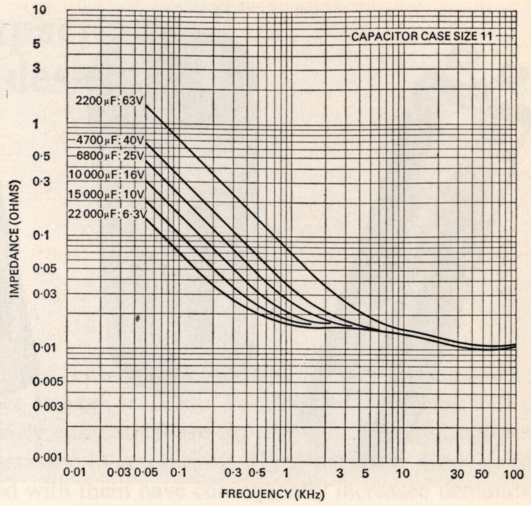


Fig. 5—Impedance as a function of operating frequency for types in can size 11

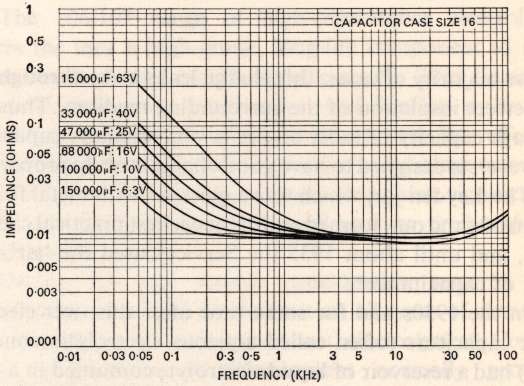
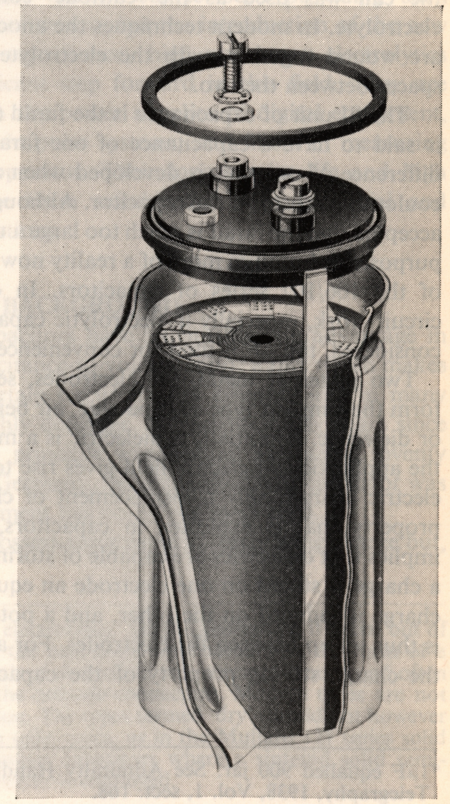


Fig. 6—Impedance as a function of operating frequency for types in can size 16



Construction of 106/107 series capacitor

CAPACITOR STRUCTURE

The description of a capacitor usually refers to the nature of its dielectric, thus an electrolytic capacitor is one where the dielectric layer is formed by electrolysis (anodic oxidation). Aluminium, vanadium, magnesium, antimony and tantalum are among those metals that are readily coated with a dielectric film by an electrolytic forming process. Satisfactory dielectric layers are formed by very thin film (of the order of a micrometre), thus giving rise to the very large capacitance/volume ratio obainable from electrolytics. The dielectric strength of such films is extremely high and in fact approaches the theoretical strength predicted by the ionic theory of crystals.

Low-voltage capacitors have thinner films and thus higher capacitance/volume ratios than high-voltage capacitors, since the maximum capacitance that can be obtained for a given anode surface area is inversely proportional to the voltage used in the forming process; that is, the forming voltage governs the thickness of the dielectric layer.

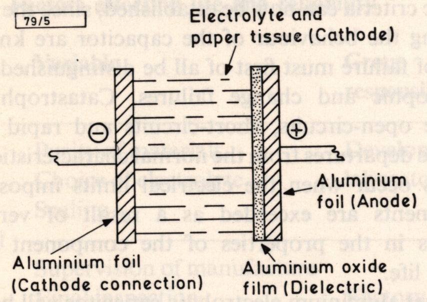

79/5
Electrolyte and paper tissue (Cathode)
⊖
⊕
Aluminium foil (Anode)
Aluminium foil (Cathode connection)
Aluminium oxide film (Dielectric)

Fig. 7—Simplified representation of electrolytic capacitor

The principal parts (Fig. 7) of a wet aluminium electrolytic capacitor, and their functions, are:

1) An etched aluminium foil, acting as the positive or anode.
2) The oxide film, which acts as the dielectric.
3) The electrolyte, which is the negative or true cathode.
4) Tissue spacers, used to absorb the electrolyte and to separate the anode and 'cathode' from direct contact.
5) Another etched aluminium foil, which acts as the contact to the electrolyte.

MANUFACTURE

The manufacture of the 106/107 series of electrolytic capacitors comprises several stages. Aluminium foil of extremely high purity is first chemically etched. This provides an effectively greater surface area and a proportionately higher capacitance. The etch-factor used is chosen to give a high capacitance per given volume whilst maintaining long-life characteristics. Some etched foil is then passed through a forming bath, which is designed so that the foil travels through a bath of electrolyte at a constant velocity and with a constant forming voltage applied, the forming voltage being higher than the specified working voltage of the capacitor. Thus the foil is immersed in electrolyte with this voltage applied for a predetermined time, enabling a controlled, predetermined dielectric film to be formed. The forming current, with constant forming voltage, falls with time as shown in Fig. 8.

Anode foil, tissue paper spacers, and 'cathode' foil are wound together on a winding machine. Since measurements are taken of the dielectric thickness, width and general properties during and after foil manufacture, the capacitance of the wound cells can be considered as a function of winding length. Thus the control on the winding and hence capacitance is kept to within specified limits.

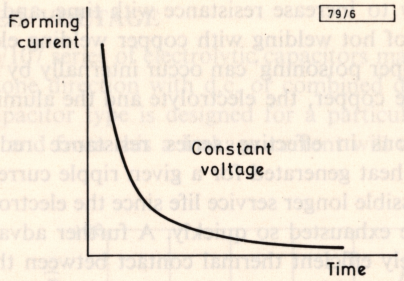


Fig. 8—Forming current as a function of time, with constant forming voltage

Connections must of course be provided for the electrodes, and these are made to the foils immediately before winding. They take the form of thick aluminium tabs cold-welded to the foil, multiple connections being made to a given length of foil.

The anode connection tabs are then cold-welded to a thick aluminium ring at one end of the cell. Similarly the 'cathode' tabs are cold-welded to a ring at the other end of the cell. Connections are then cold-welded from these rings to the underside of the screw terminals on the top of the can.

Vacuum impregnation is carried out to impregnate the cell with electrolyte. Then the cell is assembled and sealed into the can by a technique which clamps the winding in the can and ensures that the cell is in extremely good thermal contact with the can. This is a contributing factor in the high ripple current rating specified for the 106/107 series. A ring of e.p. rubber forms an extra sealing element between the top cap and the can. Compression is applied during the spin-sealing process and gives excellent proof against the vibration and bump tests experienced in some severe specifications. The can is then insulated by a plastic sleeve.

The final operation is to subject the capacitor to a prolonged period of reforming, again using a constant forming voltage.

ADVANCED SPECIFICATION OF 106/107 RANGE

High capacitance electrolytic capacitors often experience high ripple currents in service. Among the advantages produced by the research and development programme of the 106/107 series were the reduction in impedance and effective series resistance, and the increased efficiency of heat dissipation. The new type of electrolyte used reduces the ohmic resistance R_{el}, thus the overall impedance of the capacitor is less. The use of multiple connections to each electrode reduces the series resistance and is a further contributory factor to the reduced impedance since the series inductance is reduced. Low effective series resistance is further enhanced by the fact that all connections are cold-welded. This gives both an initial advantage and a long term advantage, since the resistance of connections will not increase. Other types of connection which do not give molecular bonding, as exhibited by cold-welding, are much more likely to increase resistance with time, and the disadvantage of hot welding with copper welding electrodes is that 'copper poisoning' can occur internally by reaction between the copper, the electrolyte and the aluminium.

Reductions in effective series resistance reduce the amount of heat generated for a given ripple current, thus making possible longer service life since the electrolyte will not become exhausted so quickly. A further advantage is the extremely efficient thermal contact between the capacitor winding and its can, making possible the high ripple current handling abilities of the 106/107 series.

FUNCTION AND FAILURE

During the life of the capacitor the dielectric will be slightly attacked by the liquid, but this is counteracted by the electrolytic action occurring within the capacitor when in use. Gases are released by the electrolytic action and diffuse outward through the sealing of the capacitor. In the 106/107 range a self sealing vent is provided which, even in the event of an inadvertent short term overload occurring, will release excess gas without allowing atmosphere in. The liquid electrolyte eventually becomes exhausted as a result of this process, and a gradual increase in the resistivity of the liquid occurs. Also the constituent elements of the electrolyte react, and a combination of all these phenomena physically determines the life of the capacitor.

The impedance and loss factor will increase during life (Fig. 9). The effect on the capacitance is not obvious.

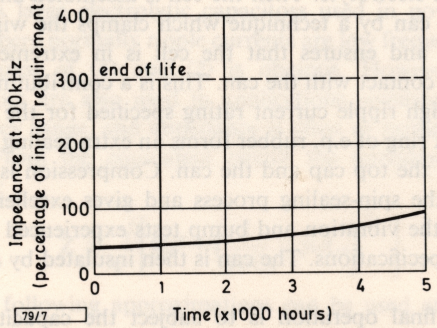


Fig. 9—Typical change of impedance during life

It can be explained by consideration of the effect of the etched surface of the anode on the total capacitance.

Total capacitance C_a is in fact made up of a number of capacitive elements. An element contained in a pore has a high series resistance by comparison with one on the surface. Fig. 3 shows a good approximation of this situation. If now the liquid resistance increases, some of the capacitive elements will lose a great deal of their effect and this will show up as a slow drop in the total capacitance after an initial rise (Fig. 10) that is attributable to the operating voltage continuing the 'forming' process. At a certain stage, the first effect outweighs the second.

The approaching end of the service life of an electrolytic capacitor is thus shown by:

1) A gradual decrease in capacitance and a related increase in impedance at 50Hz.
2) An increase in losses (tan δ).
3) An increase in the impedance at high frequencies.

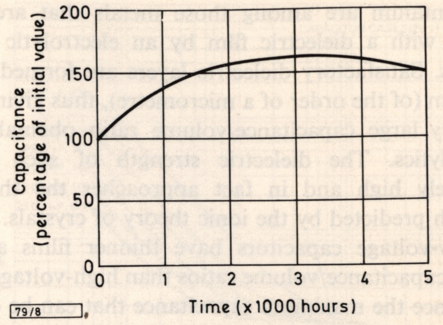


Fig. 10—Typical change of capacitance during life

REJECTION CRITERIA

Failure criteria can now be established, since the properties affecting the behaviour of the capacitor are known. Two types of failure must first of all be distinguished; these are catastrophic and change failures. Catastrophic failures include open-circuits, short-circuits and rapid or unpredictable departures from the normal characteristics. Change failures occur when the electrical limits imposed on the components are exceeded as a result of very gradual changes in the properties of the component during its service life.

A wet aluminium electrolytic capacitor will be regarded as having failed if one or more of the properties given below increases beyond the stated limits. Figures in brackets apply to capacitors with d.c. working voltages of <25V.

1) Impedance Z at 50Hz and 20°C shall not exceed 150% (200%) of the initial specified limit.
2) Dissipation factor tan δ at 50Hz and 20°C shall not exceed 200% (300%) of the initial specified limit.
3) Impedance Z at 100kHz and 20°C shall not exceed 300% of the initial specified limit.

SERVICE LIFE AND RELIABILITY

From a given batch of electrolytic capacitors (or any components, for that matter) failures will arise in service (Ref. 1). For properly manufactured, properly chosen capacitors there is a fairly constant failure rate; this gives a guide to the reliability of the component. After a certain time, gradual changes that take place in the properties of the capacitor reach a failure point evidenced by a sudden and marked increase in the total failure rate. The time that this takes to occur is a measure of the average life of the type of capacitor in question. Fig. 11 shows a curve of failure rate for wet electrolytic capacitors. It can be divided into three distinct zones.

A) Failures during manufacture and final inspection.
B) Failures during service life.
C) Failures at the end of useful life.

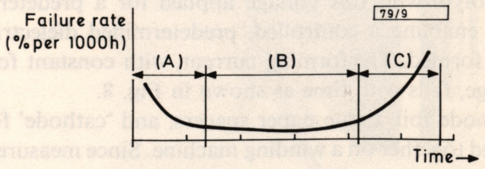


Fig. 11—Failure rate as a function of time

The service life of an electrolytic capacitor and the failure rate need not necessarily be correlated. The total area under the curve in zone B represents the total number of failures during the whole of the useful life and is generally only a small percentage of the number of capacitors under consideration. Length of service life depends to a great extent upon the design of the capacitor, the reliability of the manufacturing process, and the extent to which it is supervised and inspected.

Factors affecting the service life and reliability fall into two categories which can be called internal and external factors, as shown in the Table. Internal factors are those determined by the design of the capacitor; thus the finished product is intended for a range of applications because the designer has achieved the best compromise between the various relevant requirements. Nevertheless it is possible for the user to influence the service life and reliability by careful choice and consideration of the external factors. The effect of temperature is discussed in detail later.

Factors affecting life and reliability

Factor	Variable	Group responsible
Internal	Purity of materials Choice of electrolyte Sealing	Development laboratories
	Supervision of manufacture Final inspection Random testing	Factory
External	Temperature Voltage/current Dimensions	User

Impurities, particularly any chlorine ions, present in the materials used (aluminium foil, paper, sealing discs etc.) can cause leakage currents that accelerate the drying out process, and shorten the service life. It is therefore of prime importance that very pure materials are used and a continuous check kept on their purity.

The choice of electrolyte is nearly always a compromise between two diametrically opposed requirements. It must present a low resistance at low temperature and have only a small increase in resistance during life. A great deal of any development programme is concerned with this subject, since the overall stability of the capacitor (hence its service life) and the selected electrolyte are intrinsically joined.

One of the drawbacks of good performance at low temperatures was less favourable performance at high temperatures, but the techniques used in the 106/107 series ensure good performance over the temperature range —40° to —85°C.

Sealing of a wet electrolytic capacitor is very important, since the gases produced within the capacitor must be able to diffuse through, but the electrolyte must not leak out. The self-sealing vent used in the 106/107 series overcomes these problems extremely well.

APPLIED VOLTAGE

The 106/107 series of electrolytic capacitors may be biased only in one direction with d.c. or combined d..c and a.c. Each capacitor type is designed for a particular working voltage, and from this a leakage current will arise. It can be seen from Fig. 12 that the leakage current can be considerably reduced by reducing the applied voltage, giving increased service life. It is often asked if use at voltages lower than the specified working voltage has disadvantages. Generally, an increase in capacitance is unavoidable, but the important thing to remember is that the stability of capacitance is closely bound up with rated voltage.

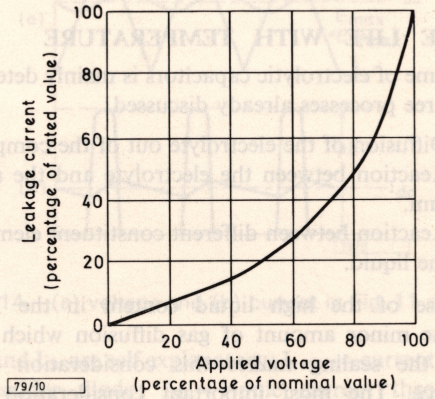


Fig. 12—Typical leakage current/applied voltage relationship

Oxide coatings designed for 25V working or more are very stable, and increases of more than 10 or 15% are seldom experienced. The thinner coatings for lower voltages, however, tend to be less stable, but these disadvantages are often outweighed by the improved service life.

QUALITY CONTROL

A vigorous and well supervised system of quality control is essential if high quality is to be maintained in the mass production of capacitors. Quality can be effectively monitored and maintained by means of the 'Q index', where

$$\text{Q index} = 100 - \left(100 \times \frac{\text{Number of penalty points}}{\text{Quantity inspected}}\right)$$

Apart from quality checks on materials and processes, 100% end of line testing is carried out for capacitance value, impedance at 100kHz, and leakage current. In addition to this, sample tests are made on the total production, testing extra electrical properties, dimensions, solderability, can damage, marking, packing and so on.

Each fault is given a weighting factor, and results of all inspections are discussed. The current Q index is considered against the past and on its own merit; thus a guide is formed and appropriate action taken to improve or maintain production quality.

An ‘A’ fault is so serious that correct working of the apparatus is endangered, a ‘B’ fault is one where under certain conditions difficulties could arise, and a ‘C’ fault is not a serious departure from the specification. An ‘A’ fault is given 100 penalty points, a ‘B’ fault 10, and a ‘C’ fault 1.

SERVICE LIFE WITH TEMPERATURE

The lifetime of electrolytic capacitors is mainly determined by the three processes already discussed:

1) Diffusion of the electrolyte out of the component.
2) Reaction between the electrolyte and the aluminium.
3) Reaction between different constituent elements of the liquid.

Because of the high liquid content in the 106/107 range, the minor amount of gas diffusion which occurs through the sealing makes this consideration of low importance. The most important consideration is the dissolution of the oxide layer. In earlier techniques with traditional glycol-based electrolytes, this phenomenon is well known. With the advanced electrolyte which is used in the 106/107 range the effect is appreciably lower, but still occurs after prolonged life. Reaction between constituent elements of the electrolyte is also very slow in this electrolyte. It does, however, vary with temperature as does the oxide breakdown. Much longer life can be expected at lower temperatures, since chemical reaction is lower.

The following are some estimated lifetimes with ambient temperature when the capacitors are used within the specification limits:

50°C	40 000 hours
60°C	23 000 hours
70°C	14 000 hours
90°C	5 000 hours

The published maximum ambient temperature limit for the 106/107 series is 85°C.

RIPPLE CURRENT AS A LIFE FACTOR

Because of the relatively high power factor of electrolytic capacitors (when compared with lower CV/volume dielectrics), the rated maximum ripple current is determined by the allowable power dissipated in the capacitor.

The power dissipation can be reduced by lowering the equivalent series resistance. As mentioned earlier, this is done with the new electrolyte employed and the multi-tab construction. As a result, the permissible ripple current is higher for this range than for others.

From a study of the effect of ripple current on service life it was concluded that temperature rise in the capacitor was the criterion. Therefore work was carried out to relate lifetime to the temperature of the electrolytic, which is a combination of ambient temperature and temperature rise due to ripple current.

Typical examples of temperature rise △T are given in the Table. They can be cross-related to service life from the preceding section, taking into account ambient temperature.

It can be seen that a small reduction in ripple current substantially reduces the temperature rise. Therefore by careful design and siting of the capacitors within the power supply, capacitor life can be considerably increased.

Temperature rise and ripple current

Can size	Voltage rating (V)	△T= 5degC	△T= 15degC	△T= 25degC	△T for capacitor run at 20% of I_R max. (degC)
		Ripple current (A)	Ripple current (A)	Ripple current (A)	
11	6·3 to 25V	5·2	9·0	11·7	0·4
	40 to 100V	4·6	8·1	10·4	0·5
14	6·3 to 25V	7·3	12·6	16·3	0·6
	40 to 100V	6·4	11·1	14·3	0·7
16	6·3 to 25V	13·3	23·1	29·8	0·9
	40 to 100V	11.8	20·4	26·3	1·1

DATA AND PERFORMANCE

Brief electrical data: for 106/107 range:

CV product (capacitance times normal working voltage)	Up to one farad.volt. Actual values of capacitance and voltage are given in Fig. 1.
Ripple current at 50°C	7 to 28A dependent on can size.
Impedance at 100kHz	0·05 to 0·1Ω dependent on can size.
Leakage current	0·006 CV (C in μF, V in volts).
Typical effective series inductance	0·2 to 0·5μH dependent on can size.

Post Office approved to specification D2186
Ministry of Defence (Navy Dept) approved to specification DEF 5134–1.

Typical drift, 6800μF 40V capacitor

	0 hours	*5000 hours*
C at 50Hz	7000μF	6200μF
tan δ at 50Hz	2·7%	4·8%
Z at 100kHz	0·027Ω	0·029Ω
Leakage current	140μA	130μA

TYPICAL APPLICATION

A single-phase full-wave bridge rectifier circuit, with a capacitor input filter (Fig. 13) is a typical application for the 106/107 series, especially if the load current, and therefore the ripple current, is high.

The capacitor C will store energy when the applied voltage E_T is in excess of the terminal voltage of the capacitor, and deliver energy to the load when E_T is below the terminal voltage. The idealised waveforms after steady state has been established are shown in Fig. 14. Smoothing is more efficient in a full-wave circuit than in a half-wave circuit, since the capcitor maintains the load current over a shorter period and therefore the capacitor voltage change will be smaller.

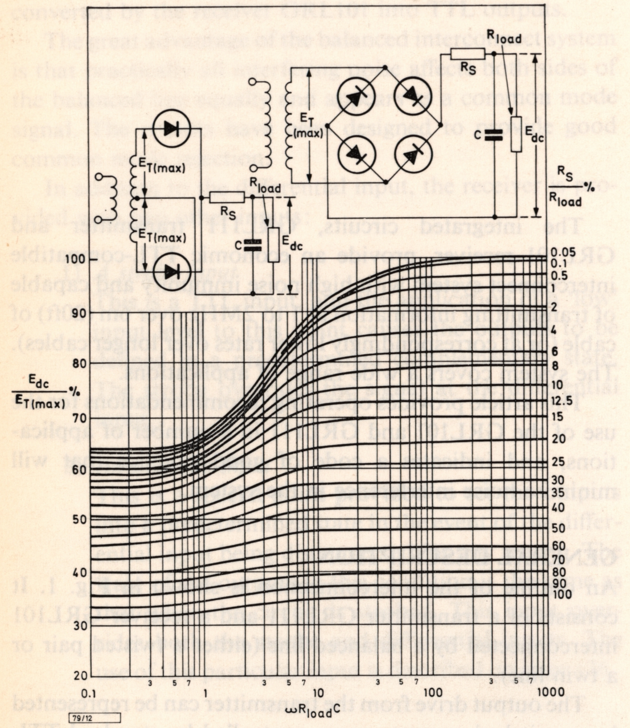


Fig. 13—Single-phase full-wave bridge rectifier, with E_{dc}/E_{Tmax} % as a function of wR $_{LOAD}$ C where C is in farads and R $_{LOAD}$ is in ohms

The capacitor used in the circuit must be rated to withstand the working voltage $E_{dc}+\Sigma_R$, and the ripple current which will flow through the circuit:

$$I_{R(rms)} = \sqrt{(2I_{rms}^2 - I_{dc}^2)}$$

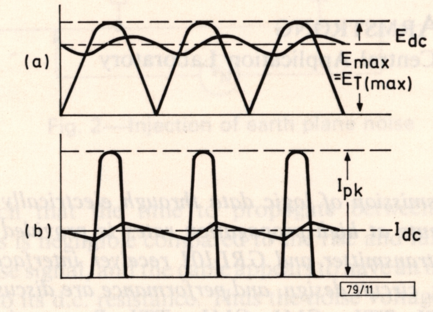


Fig. 14—(a) voltage and (b) current in Fig. 11 circuit

E_{dc} and I_{dc} are self explanatory; I_{rms} = current through each rectifier diode; I_R = ripple current through the capacitor; Σ_R is the sum of any a.c. voltages appearing across the capacitor.

At initial switch-on large currents can flow since the charge in the capacitor may be low. Therefore the source resistance must be a compromise between lost efficiency—thus poor regulation—and the peak current rating of the rectifiers.

Design procedure is simplified by using the graphical method given in Ref. 2 and Ref. 3.

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TTL interfacing with GRL111 and GRL101

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Fast transmission of logic data through electrically hostile environments at high propagation rates is provided by the GRL111 transmitter and GRL101 receiver interface units. Principles, circuit design, and performance are discussed for TTL—TTL, TTL—CML, CML—TTL. Propagation at up to 20MHz with a minimum noise immunity of 12V pk-pk can be achieved.

INTRODUCTION

There exists in many logic systems a requirement for transmitting data from one piece of digital equipment to another through what might be an electrically hostile environment. At the same time it may be required to transmit the data at a maximum rate. These can be conflicting requirements.

The electrical interference may be produced by almost any conceivable electrical device and have components in the frequency spectrum from zero upwards. The most significant noise components are at d.c., 50Hz (the supply frequency), and harmonics of 50Hz. The sources of this interference are earth return circuits and direct radiation from mains-fed equipment including cables.

Other forms of noise include spike interference from similar nearby circuits, power switching in nearby equipment, and interference from local transmitters.

In a wide range of digital equipment the logic will be performed by TTL circuits. These circuits have an adequate noise margin when operating within the confines of an equipment, but in most cases the noise margin will not be adequate for interconnections from equipment to equipment. A requirement therefore exists for a high-noise-immunity interconnect system which can interface with TTL at both ends of the interconnection.

The integrated circuits, GRL111 transmitter and GRL101 receiver, provide an economic TTL-compatible interconnect system with high noise immunity and capable of transmitting information at 1 to 2MHz over 6m (20ft) of cable (or at correspondingly lower rates over longer cables). The system covers a wide range of applications.

This article provides operating recommendations for the use of the GRL101 and GRL111 in a number of applications, and indicates a code of good practice that will minimise noise interference in the system.

GENERAL DESCRIPTION

An outline of the interconnection is shown in Fig. 1. It consists of a transmitter GRL111 and a receiver GRL101 interconnected by a balanced line (either a twisted pair or a twin line).

The output drive from the transmitter can be represented by a switched current source controlled by standard TTL switching levels. The receiver converts the differential signals to TTL outputs, both the 'true' and 'false' polarities being provided.

In the transmitter the current of nominal value 14mA is switched from output A to B and vice versa in response to TTL signals at the input. This gives the effect of a differential current to the line of 14mA.

The signal generated will propagate along the cable to the receiving end, where it is correctly terminated in a differential termination. Since most differential cables in use at the present time have a characteristic impedance of about 100Ω, the GRL111 and GRL101 have been developed for use with this value. A correctly terminated system enables the maximum speed of operation to be realised. The speed is limited by the propagation delay t_d of the cable (up to about 6½ns per metre run of cable or 2ns per foot) and the propagation delay of the circuits at the ends of the cable.

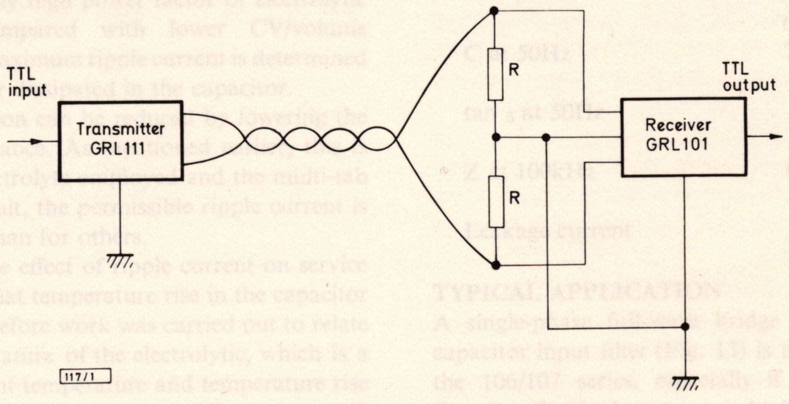

Fig. 1—Simple interconnect system

The differential signal current in the cable produces a differential voltage signal at the termination which is converted by the receiver GRL101 into TTL outputs.

The great advantage of the balanced interconnect system is that practically all interfering noise affects both sides of the balanced line equally and appears as a common mode signal. The circuits have been designed to provide good common mode rejection.

In addition to the differential input, the receiver is provided with two other inputs:

1) *A strobe input*
This is a TTL input, and the application of a 'low' input level to this point causes the outputs to be defined in a predetermined complementary state. The strobe overrides the signal at the differential input.

2) *An override input*
This is a special point provided to set the outputs into a predetermined state in the event of the differential input being disconnected for any reason. The state of the outputs in this condition is the same as that when the circuit is strobed. This input overrides both the strobe and differential inputs. The use of this particular input is described on page 136.

NOISE

The interconnection system described will provide a good performance in an electrically noisy environment, at a propagation rate limited only by the propagation delay of the cable and of the circuits.

This section discusses the various forms of noise that arise in the interconnect system, and how they will be handled by the system.

Earth plane noise

In any electrically connected system there is likely to be a voltage set up between the separate earth planes of the system. The main components of this noise will be at d.c. and at 50Hz (the local supply frequency). These noise voltages are attributable to

1) The finite impedance between the point at which the signal input/output is referenced and the point in the equipment where the main earth connection is made.
2) The finite impedance in the earth connections between the two interconnected equipments.
3) Coupling between the mains supply wiring and the earth interconnect systems.

In Fig. 2, V_N represents the voltage between the two earth planes. A circulating current will flow which is dependent on the magnitude of the terminating resistors and the effective d.c. impedance of the line. The frequencies are such that the time to propagate between the two systems is negligible compared to the rise and fall times of the noise signal, and the cable appears to have an impedance equal to its d.c. resistance. Thus the noise voltage that will appear as a common mode signal at the transmitter is given by

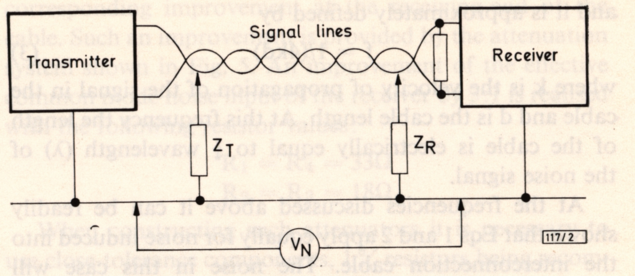

Fig. 2—Injection of earth plane noise

$$V_{NT} = \frac{Z_T}{Z_T+Z_R} \cdot V_N \qquad \ldots(1)$$

and at the receiver by

$$V_{NR} = \frac{Z_R}{Z_T+Z_R} \cdot V_N \qquad \ldots(2)$$

where Z_T and Z_R are the common mode terminations presented at the transmitting and receiving ends of the cable respectively.

In the arrangement shown in Fig. 1, $Z_T = \infty$ and Z_R is equal to one quarter of the differential termination (it is simply the two halves of the termination in parallel). The situation then exists that to a first approximation the whole of V_N appears at the transmitter and none at the receiver.

The transmitter therefore has to be designed to cope with the whole of the voltage V_N. The GRL111 has been designed to handle a minimum of ±6V (12V peak-to-peak) over the full range of temperature and supply variations. For most applications this will give adequate noise margins without elaborate precautions.

For systems where this noise performance is not expected to be sufficient, the following precautions should be observed:

1) The impedance from the signal cable input earth to the main earth should be minimised.
2) The earth impedance between the two equipments should be minimised.
3) Circulating currents in earth return systems should be avoided.
4) Mains supply cable routeing should not be too close to the earthing cables.
5) Where possible, the use of stout braiding in earthing connections should be considered.

Although the foregoing discussion has been centred on two particular noise frequencies (d.c. and 50Hz) the arguments apply equally to higher frequencies. The limiting frequency is that at which the time to propagate down the cable is a significant portion of the cycle time of the noise, and it is approximately defined by

$$f = 1/(4kd) \qquad \ldots(3)$$

where k is the velocity of propagation of the signal in the cable and d is the cable length. At this frequency the length of the cable is electrically equal to $\frac{1}{4}$ wavelength (λ) of the noise signal.

At the frequencies discussed above it can be readily shown that Eqs 1 and 2 apply equally for noise induced into the interconnection cable. The noise in this case will therefore appear wholly at the transmitter.

Common mode noise injected into line

The cable will normally have an electrostatic shield that is an overall sheath to minimise direct pick-up.

We have so far discussed earth plane noise and have included under that general heading all noise frequencies less than f in the equation $f = 1/(4kd)$, where the cable can be considered as not behaving as a transmission line. Higher noise frequencies cannot be treated in so simple a manner. Noise frequencies satisfying the approximate formula

$$f > 1/(4kd) \qquad \ldots(4)$$

will appear at the ends of the cable in a manner dependent on the terminations and the distribution of the noise in the cable.

In the simple case where the noise is injected at the centre of the line, the relevant impedances can be represented by the system of Fig. 3. The voltage V_T appearing

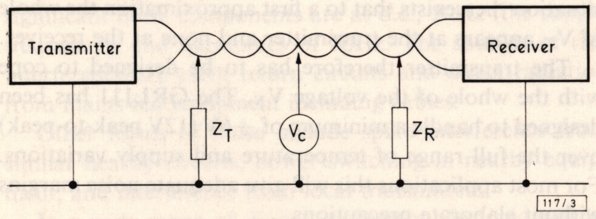

Fig. 3—Injection of line noise

at a termination Z_t as a result of a voltage V_C in a cable of characteristic impedance Z_0 is given by the normal reflection equation

$$V_T = 2Z_t/(Z_t+Z_0) \qquad \ldots(5)$$

where Z_t and Z_0 are the common mode terminating impedance and cable characteristic impedance respectively.

In the simple case of Fig. 1, where $Z_T = \infty$ and $Z_R = 25\Omega$* the noise voltage at the receiver is

$$V_{TR} = \frac{50}{25+175} \,.\, V_c = V_c/4.$$

The assumed common mode impedance Z_0 of 175Ω for the cable is a realistic figure for practical cables.

At the transmitter the noise voltage is

$$V_{TT} = 2V_c.$$

Thus the ratio of noise at the two ends of the cable is 8:1, the larger figure being at the transmitter.

In the foregoing discussion two practical assumptions have been made.

1) Noise appearing in a common mode sense in the cable will be quickly attenuated, therefore reflections due to improper common mode terminations do not have to be considered. Experiment has shown that with a length of only 6 metres of multi-core computer cable the effect of the common mode termination was minimal on the noise appearing at the other end of the cable.
2) Noise can be considered as being injected at the centre of the cable.

The GRL111 transmitter has been developed to accept a minimum of 12V peak-to-peak of noise, while under the worst operating conditions the GRL101 receiver can accept at least a minimum of 1·5V peak-to-peak of common mode noise at its input. The layout shown in Fig. 1 therefore forms a very useful interconnect system in which the noise immunity of the transmitter and of the receiver are compatible.

For use in exceptionally noisy environments the noise immunity of the basic interconnect system can be improved by the use of the system shown in Fig. 3. The common mode termination impedance at the transmitter, instead of being infinite, is chosen to have a value equal to the characteristic impedance of the cable. The noise voltage at the transmitter in this situation is, from the reflection equations:

$$V_{TT} = \frac{2Z_0}{Z_0+Z_0} \,.\, V_c = V_c. \qquad \ldots(6)$$

Thus by having a common mode termination at the transmitter, the high-frequency noise immunity of this end of the cable is improved by a factor of 2 over the simple interconnect system.

A practical method of connecting a common mode termination is shown in Fig. 4. The common mode impedance Z_0 (≃175Ω) will be matched by the two resistors

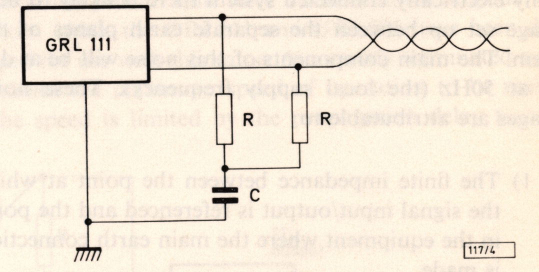

Fig. 4—Practical common-mode termination $R = 2.Z_0$

in parallel, thus R = 330Ω (nearest preferred value). The impedance presented differentially to the line (2R = 660Ω) is much higher than the differential impedance (about 100Ω) of the cable, and will not therefore have any significant effect on the differential signal. The capacitor C is included so that the common mode termination will not interfere with the low-frequency noise immunity. A value of 100nF will be adequate for use with cables up to 150m (500ft) in

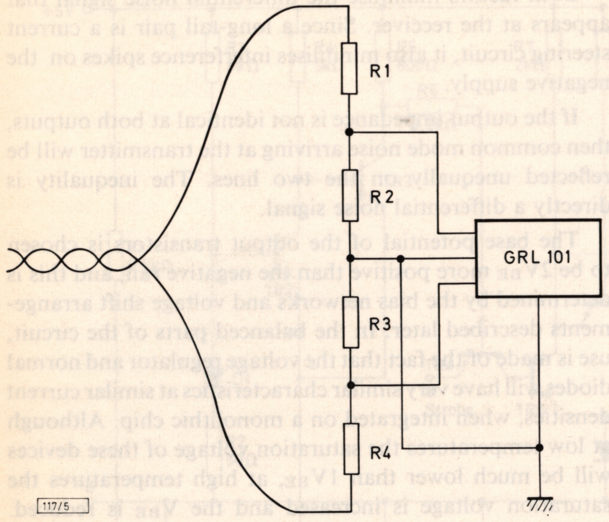

Fig. 5—Differential attenuator
$R_1 = R_4 \quad R_2 = R_3$
$R_1+R_2+R_3+R_4 = Z_{diff}$ (the differential impedance of the cable)

length. For longer cables the frequencies for which the cable is electrically long are decreased as the inverse of the cable length. Capacitor C has therefore to be increased in proportion (that is, by 200nF for every 300m).

To make full use of the improved noise immunity at the transmitter end of the cable it is necessary to provide a corresponding improvement at the receiving end of the cable. Such an improvement is provided by the attenuation system shown in Fig. 5. An improvement of the effective common mode noise input of the receiver by 3:1 is realised with the following resistor values:

$$R_1 = R_4 = 33\Omega$$
$$R_2 = R_3 = 18\Omega\,.$$

When constructing such attenuators it is necessary to use close-tolerance components, 1% resistors being recommended. This is because an effective differential signal can result at the receiver terminals because of the action of a common mode signal on the differential tolerances of the attenuator network. This effect is fully explained on page 136.

TRANSMITTER CIRCUIT

The circuit of the GRL111 transmitter is given in Fig. 6. The circuit can be divided into four sections for the purposes of description:

1) Input circuit TR_1 to TR_7 and D_1 to D_3.
2) Output circuit TR_{10} and TR_{13} with overvoltage protection components D_6 to D_9.
3) Voltage—shifting and phase-splitting network TR_8, TR_9, TR_{11}, TR_{14} to TR_{16} and D_4, D_5, D_{10}, D_{11}.
4) Biasing and current generator networks TR_{12}, TR_{17}, TR_{19}, D_{12} to D_{19}.

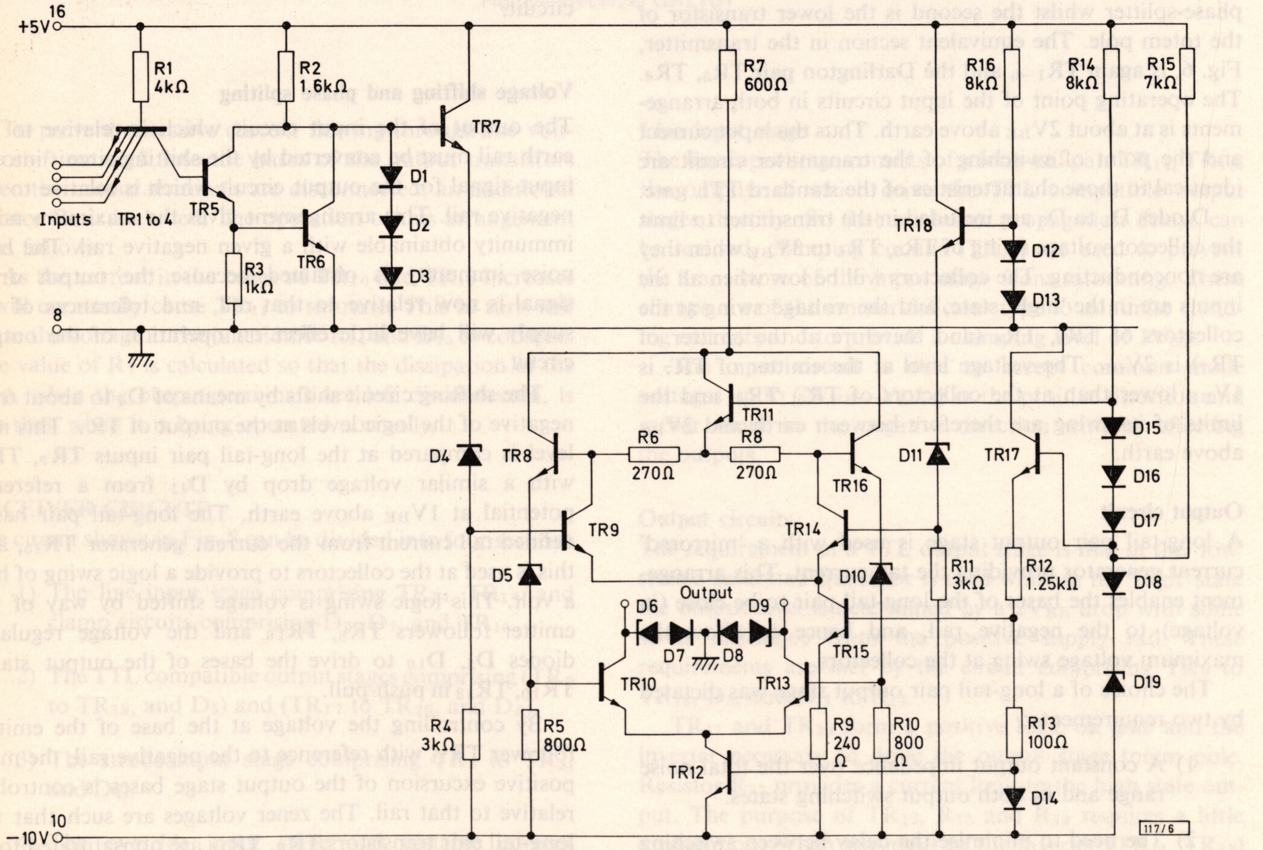

Fig. 6—Transmitter GRL111

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*The recommended differential termination for the interface system is 100 Ω.

Input section

The transmitter is mainly intended to be used in conjunction with TTL circuits. It is desirable, therefore, that the input characteristics of the transmitter are identical to those of a standard TTL gate. A normal TTL gate, Fig. 7, has an input stage consisting of an input transistor TR$_{1-4}$ whose collector is directly coupled to a cascaded pair of transistors TR$_5$, TR$_6$. The first transistor of the pair forms the phase-splitter whilst the second is the lower transistor of the totem pole. The equivalent section in the transmitter, Fig. 6, is again TR$_{1-4}$, and the Darlington pair TR$_5$, TR$_6$. The operating point of the input circuits in both arrangements is at about 2V_{BE} above earth. Thus the input current and the point of switching of the transmitter circuit are identical to those characteristics of the standard TTL gate.

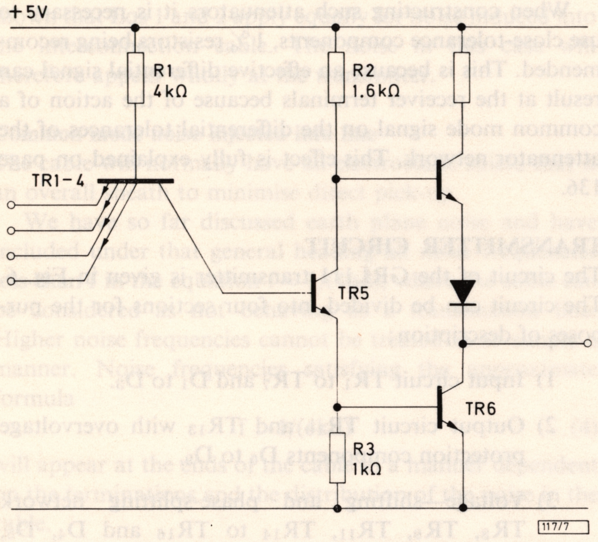

Fig. 7—Standard TTL NAND gate

Diodes D$_1$ to D$_3$ are included in the transmitter to limit the collector voltage swing of TR$_5$, TR$_6$ to 3V_{BE} when they are nonconducting. The collectors will be low when all the inputs are in the 'high' state, and the voltage swing at the collectors of TR$_5$, TR$_6$ (and therefore at the emitter of TR$_7$) is 2V_{BE}. The voltage level at the emitter of TR$_7$ is 1V_{BE} lower than at the collectors of TR$_5$, TR$_6$, and the limits of its swing are therefore between earth and 2V_{BE} above earth.

Output circuit

A long-tail pair output stage is used with a 'mirrored' current generator providing the tail current. This arrangement enables the bases of the long-tail pair to be close (in voltage) to the negative rail, and hence to allow the maximum voltage swing at the collectors.

The choice of a long-tail pair output stage was dictated by two requirements:

1) A constant output impedance over the total noise range and in both output switching states.

2) The need to minimise the delay between switching at the two outputs.

Both factors minimise the differential noise signal that appears at the receiver. Since a long-tail pair is a current steering circuit, it also minimises interference spikes on the negative supply.

If the output impedance is not identical at both outputs, then common mode noise arriving at the transmitter will be reflected unequally on the two lines. The inequality is directly a differential noise signal.

The base potential of the output transistors is chosen to be 2V_{BE} more positive than the negative rail, and this is determined by the bias networks and voltage shift arrangements described later. In the balanced parts of the circuit, use is made of the fact that the voltage regulator and normal diodes will have very similar characteristics at similar current densities, when integrated on a monolithic chip. Although at low temperatures the saturation voltage of these devices will be much lower than 1V_{BE}, at high temperatures the saturation voltage is increased and the V_{BE} is reduced. Therefore at excessive temperatures the current generator, by saturating, can help to avoid the condition of thermal runaway by reducing the output current. Since the output circuit is being driven in push-pull, an output differential can still be available even at elevated temperatures, although there will be an increased common mode component and reduced output current.

Voltage breakdown of the output devices, caused by line surges in the positive direction, is avoided by the use of the four diodes D$_6$ to D$_9$. In the reverse direction, protection is effected by the forward conduction of the base-collector junction and the low impedance of the base circuit.

Voltage shifting and phase spliting

The output of the input circuit which is relative to the earth rail must be converted by the shifting circuit into an input signal for the output circuit which is relative to the negative rail. This arrangement gives the maximum noise immunity obtainable with a given negative rail. The high noise immunity is obtained because the output drive signal is now relative to that rail, and tolerances of the supply will have little effect on operation of the output circuit.

The shifting circuit shifts by means of D$_4$ to about 6·5V negative of the logic levels at the output of TR$_7$. This new level is compared at the long-tail pair inputs TR$_9$, TR$_{14}$ with a similar voltage drop by D$_{11}$ from a reference potential at 1V_{BE} above earth. The long-tail pair has a defined tail current from the current generator TR$_{15}$, and this is used at the collectors to provide a logic swing of half a volt. This logic swing is voltage shifted by way of the emitter followers TR$_8$, TR$_{16}$ and the voltage regulator diodes D$_5$, D$_{10}$ to drive the bases of the output stages TR$_{10}$, TR$_{13}$ in push-pull.

By controlling the voltage at the base of the emitter follower TR$_{11}$ with reference to the negative rail, the most positive excursion of the output stage bases is controlled relative to that rail. The zener voltages are such that the long-tail pair transistors TR$_9$, TR$_{14}$ are nonsaturated for a wide range of negative voltages ($>\pm10\%$).

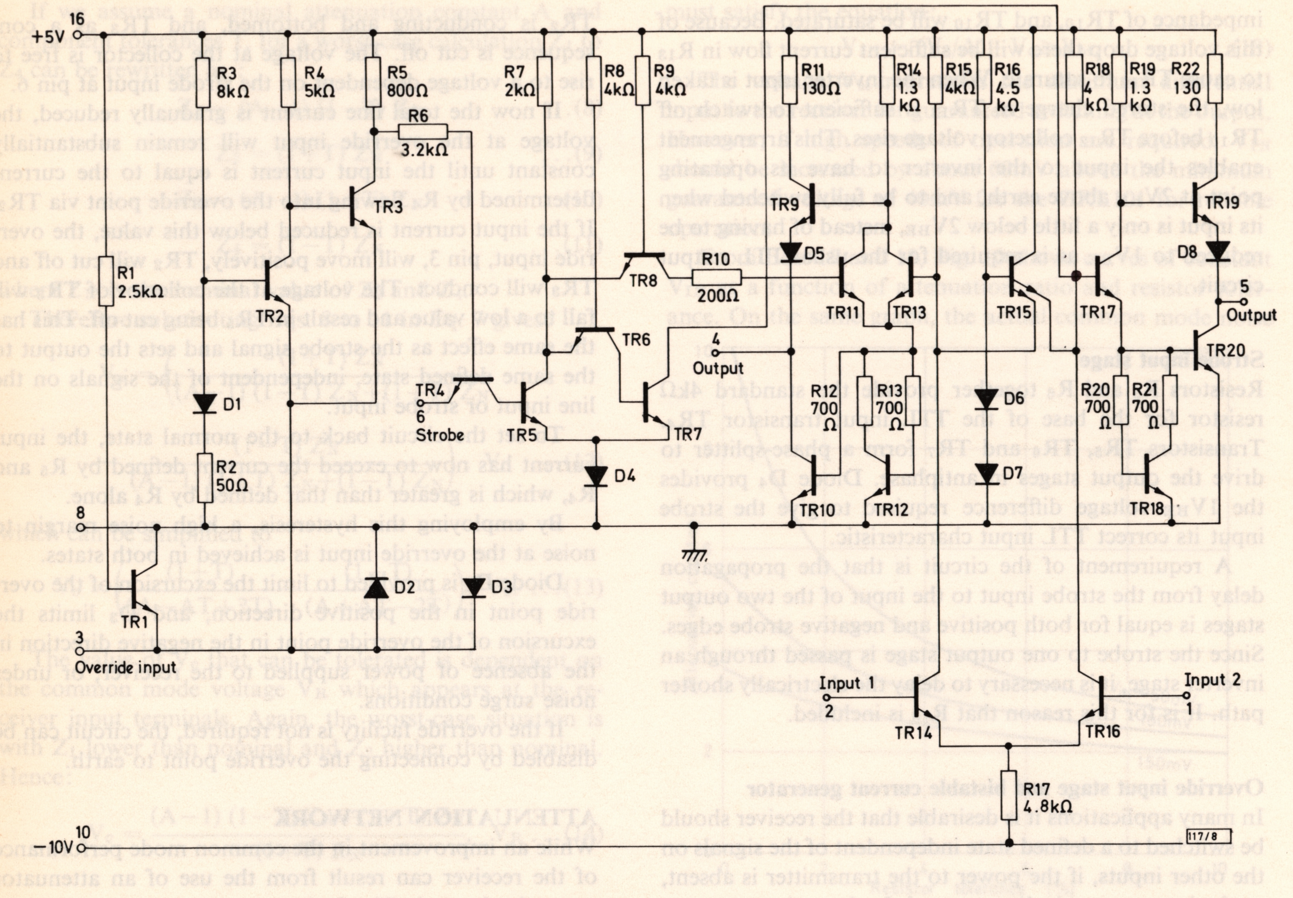

Fig. 8—Receiver GRL101

To prevent excessive current flowing through the voltage shift network into the bases of the output transistors when the output terminals are disconnected, an additional resistor R$_7$ is included. The operation of this arrangement is as follows.

As the current in the bases of TR$_{10}$ and TR$_{13}$ increases it will eventually cause TR$_{11}$ to saturate. This in turn will cause the voltage at the junction of R$_{14}$ and D$_{15}$ to collapse. The value of R$_7$ is calculated so that the dissipation of the chip, when the output terminals are left disconnected, is less than when it is being operated normally.

RECEIVER CIRCUIT

The circuit shown in Fig. 8 can be divided into four sections

1) The line input stage comprising TR$_{14}$, TR$_{16}$, and clamp circuits comprising D$_6$, D$_7$, and TR$_{15}$.

2) The TTL compatible output stages comprising (TR$_9$ to TR$_{13}$, and D$_5$) and (TR$_{17}$ to TR$_{20}$, and D$_8$).

3) The strobe input stage comprising TR$_4$ to TR$_8$, and D$_4$).

4) The override input stage and bistable current generator comprising TR$_1$ to TR$_3$, and D$_1$ to D$_3$.

Line input stage

The line input stage consists of a long-tail pair TR$_{14}$, TR$_{16}$, the outputs of which drive the TTL compatible output stages directly. So that minimum propagation delays can be realised, clamping circuits (TR$_{15}$) are used to prevent the transistors of the input stage from saturating. These clamps are of the emitter-follower type to minimise standing currents and to provide a clamping level of 1V_{BE}.

The input circuit is able to accept common mode voltages up to $(2V_{BE}-V_{knee})$ in the positive direction and rather more in the negative direction without affecting the outputs.

Output circuits

The requirement of a TTL output stage is that in the 'low' state a saturated transistor is used while in the 'high' state the output level is determined by a 2V_{BE} drop with some series resistance from the positive supply rail. These requirements are met by the circuit comprising TR$_9$ to TR$_{13}$, D$_5$, and R$_{11}$ to R$_{14}$.

TR$_{11}$ and TR$_{13}$ form a positive logic OR gate and the inverter necessary to drive the output stage totem pole. Resistor R$_{11}$ provides a current limit to the high state output. The purpose of TR$_{12}$, R$_{12}$ and R$_{13}$ requires a little explanation. When the input to the inverter (TR$_{11}$, TR$_{13}$) is high, there will be a voltage drop at the base input impedance of TR_{10}, and TR_{10} will be saturated. Because of this voltage drop there will be sufficient current flow in R_{13} to cause TR_{12} to saturate. When the inverter input is taken low, the stored charge in TR_{12} is sufficient to switch off TR_{10} before TR_{12} collector voltage rises. This arrangement enables the input to the inverter to have its operating point at $2V_{BE}$ above earth, and to be fully switched when its input is only a little below $2V_{BE}$, instead of having to be reduced to $1V_{BE}$ as is required for the usual TTL output circuit.

Strobe input stage

Resistors R_5 and R_6 together provide the standard 4kΩ resistor for the base of the TTL input transistor TR_4. Transistors TR_5, TR_6 and TR_7 form a phase-splitter to drive the output stages in antiphase. Diode D_4 provides the $1V_{BE}$ voltage difference required to give the strobe input its correct TTL input characteristic.

A requirement of the circuit is that the propagation delay from the strobe input to the input of the two output stages is equal for both positive and negative strobe edges. Since the strobe to one output stage is passed through an inverter stage, it is necessary to delay the electrically shorter path. It is for this reason that R_{10} is included.

Override input stage and bistable current generator

In many applications it is desirable that the receiver should be switched to a defined state independent of the signals on the other inputs, if the power to the transmitter is absent, or the interconnect is disconnected. In these circumstances the override circuit ensures that output 1 goes 'high' and output 2 goes 'low'. This facility may be employed, or not, at the choice of the logic designer.

If the override is employed, the override input is connected to the centre tap of the differential termination and acts as a virtual earth. The total line current then flows into this point, and is measured to determine whether it is above, or below, one of two levels. One level (2mA nominal) is used when the line current falls from its normal steady value toward zero; the other (6mA nominal) when it rises from zero to its steady state. The two levels are chosen to give the maximum noise margin in either state (on or off).

Each of the two levels will have a tolerance from device to device; thus if the line current is assumed to be decreasing from its nominal value, no circuit will switch to the defined state until the line current has fallen below 2·5mA. However, the current must fall below 0·5mA to ensure that all circuits have switched. Again, with the current rising all circuits will remain in the defined state until 3·5mA, and every circuit will have switched to the normal operating condition with an input current of 8·5mA.

The override circuit consists of TR_1 to TR_3 and D_1 to D_3. In normal operation the total line current is fed to point 3 and then mainly through TR_1 to earth. Under these conditions TR_1 is bottomed and point 3 is at V_{CEsat} of TR_1 below the earth rail. The bias to the base of TR_2 is set to a nominal value ($1V_{BE}+50mV$) by means of the network R_2, R_3, and D_1. Thus in normal operating conditions TR_2 is conducting and bottomed, and TR_3 as a consequence is cut off. The voltage at the collector is free to rise to a voltage dependent on the strode input at pin 6.

If now the total line current is gradually reduced, the voltage at the override input will remain substantially constant until the input current is equal to the current determined by R_4 flowing into the override point via TR_2. If the input current is reduced below this value, the override input, pin 3, will move positively, TR_2 will cut off and TR_3 will conduct. The voltage at the collector of TR_3 will fall to a low value and result in TR_5 being cut off. This has the same effect as the strobe signal and sets the output to the same defined state, independent of the signals on the line input or strobe input.

To set the circuit back to the normal state, the input current has now to exceed the current defined by R_5 and R_4, which is greater than that defined by R_4 alone.

By employing this hysteresis, a high noise margin to noise at the override input is achieved in both states.

Diode D_2 is provided to limit the excursion of the override point in the positive direction, and D_3 limits the excursion of the override point in the negative direction in the absence of power supplied to the receiver, or under noise surge conditions.

If the override facility is not required, the circuit can be disabled by connecting the override point to earth.

ATTENUATION NETWORK

While an improvement in the common mode performance of the receiver can result from the use of an attenuator network, shown in Fig. 9, there are consequent reductions in differential noise margins, for two reasons:

1) There is a direct attenuation of the differential signal.
2) Differential tolerances of the attenuator components cause common mode signals to result in differential signals.

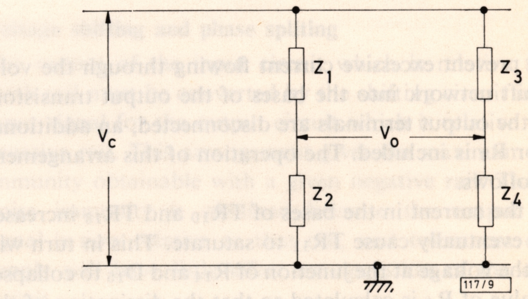

Fig. 9—Attenuator network

The second effect emphasises the need for close-tolerance components. The following worst-case calculation explains the effect.

In Fig. 9 the output voltage V_o developed as a result of a common mode input signal V_c can be written:

$$V_o = \left(\frac{Z_2}{Z_1+Z_2} - \frac{Z_4}{Z_3+Z_4}\right). V_c. \qquad \ldots(7)$$

If we assume a nominal attenuation constant A and component tolerances T, for a worst-case calculation Z_1 to Z_4 can be rewritten as :

$$Z_1 = (A-1)(1-T)Z_N \qquad \ldots(8)$$

$$Z_2 = (1+T)Z_N \qquad \ldots(9)$$

$$Z_3 = (A-1)(1+T)Z_N \qquad \ldots(10)$$

$$Z_4 = (1-T)Z_N \qquad \ldots(11)$$

where Z_N is the nominal value of Z_2 and Z_4.

Therefore substituting Eqs. 8 to 11 in Eq. 7 gives:

$$V_o = \left(\frac{(1+T)Z_N}{(A-1)(1-T)Z_N+(1+T)Z_N} - \frac{(1-T)Z_N}{(A-1)(1+T)Z_N+(1-T)Z_N}\right). V_c \qquad \ldots(12)$$

which can be simplified to

$$V_o = \left(\frac{(1+T)}{(A-AT+2T)} - \frac{(1-T)}{(A+AT-2T)}\right). V_c. \qquad \ldots(13)$$

The value of V_c that can be tolerated is dependent on the common mode voltage V_R which appears at the receiver input terminals. Again, the worst-case situation is with Z_1 lower than nominal and Z_2 higher than nominal. Hence:

$$V_c = \frac{(A-1)(1-T)Z_N+(1+T)Z_N}{(1+T)Z_N}. V_R \qquad \ldots(14)$$

which can be simplified to

$$V_c = \frac{(A-AT+2T)}{(1+T)}. V_R. \qquad \ldots(15)$$

Substitution in Eq. 13 gives

$$V_o/V_R = \frac{4T(A-1)}{(A-AT+2T)(A+AT-2T)} \cdot \frac{(A-AT+2T)}{(1+T)} \quad (16)$$

which can be simplified to

$$V_o/V_R = \frac{4T(A-1)}{(A+AT-2T)(1+T)} \cdot \qquad \ldots(17)$$

The value of V_R for the GRL101 is ±0·7V in the worst case. Again, in the worst case situation, the value of V_o in Eq. 17 will subtract from the attenuated differential input voltage V_S/A at the receiver input terminals. If the minimum guaranteed window voltage is V_M, then for correct operation of the receiver the input differential input V_{IN} must satisfy the equation:

$$V_{IN} = (V_S/A) - V_o \geqslant V_M. \qquad \ldots(18)$$

The voltage V_M represents the minimum differential input to the receiver for guaranteed switching at the output. However, if high speeds of operation are required, V_{IN} should be increased by about 60mV above the minimum guaranteed voltage of 40mV for the GRL101 for reliable operation.

From Eqs. 17 and 18, Fig. 10 shows curves of constant V_{IN} as a function of attenuation ratio and resistor tolerance. On the same graph, the actual common mode noise immunity can be calculated from Eq. 15, which can be simplified for small T to:

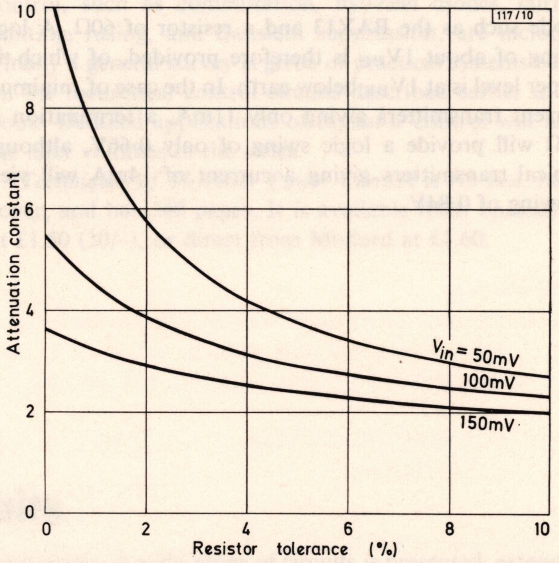

Fig. 10—Constant V_{IN} as a function of attenuation ratio and resistor tolerance
V_s = 0·55V for worst-case transmitter
where I = 11mA and Z_{diff} = 100Ω

$$V_c = \pm A.V_R. \qquad \ldots(19)$$

For the GRL101, V_R=0·7V hence

$$V_c = \pm 0{\cdot}7V \times A \qquad \ldots(20)$$

or

$$V_c = 1{\cdot}4 \times A \text{ volts peak to peak.} \qquad \ldots(21)$$

INTERFACING WITH CML

The GRL111 and GRL101 interface circuits can be used to interface with CML (such as MECL) with a minimum of additional components.

TTL to CML interface

In Fig. 11, one output of the GRL111 is returned to earth, and the other is returned to earth through a silicon

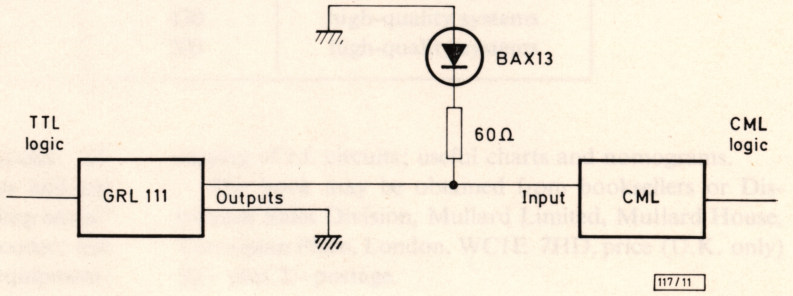

Fig. 11—TTL-CML interface

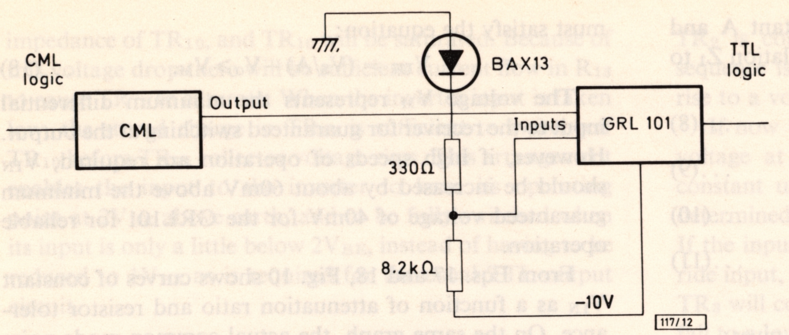

Fig. 12—CML-TTL interface

diode such as the BAX13 and a resistor of 60Ω. A logic swing of about $1V_{BE}$ is therefore provided, of which the upper level is at $1V_{BE}$ below earth. In the case of minimum current transmitters giving only 11mA, a termination of 60Ω will provide a logic swing of only 0·66V, although typical transmitters giving a current of 14mA will yield a swing of 0·84V.

CML to TTL interface

In Fig. 12, the GRL101 can be used to convert CML levels to TTL levels. The line inputs to the GRL101 receiver should be connected one to the output of the CML circuit, and one to a suitable bias point at $1\frac{1}{2}V_{BE}$ below earth. A suitable bias network using a silicon diode BAX13 is indicated in the figure.

Power Engineers using Thyristors

A new series of books for electrical and electronic engineers

The introduction of thyristors and other semiconductor power devices has brought many changes to the electrical industry. In particular, the once apparently rigid division between electronics and power engineering is now a thing of the past. Electrical engineers must now know about electronic control techniques, while electronic engineers must now think about circuits handling megawatts.

There is at present a shortage of textbooks on thyristor power control. Mullard are therefore introducing a new series to cover this 'hybrid' subject. The series is called *Power Engineering Using Thyristors,* and the first volume—*Techniques of Thyristor Power Control*—is now available.

Techniques of Thyristor Power Control is concerned with the thyristor and the way in which it can be used in control circuits. Starting with a brief description of the thyristor and its characteristics, basic control circuits are discussed. Chapters on aspects common to all applications of thyristor control, such as commutation, flywheel diodes, current limiting, fusing, and transient suppression, are included. Finally a general survey is given of practical systems based on the theoretical control circuits described earlier in the book. Detailed applications of thyristor control will form the later volumes in the series.

Techniques of Thyristor Power Control is A5 size, hardcover, and has 240 pages. It is available from booksellers at £1.50 (30/–), or direct from Mullard at £1.60.

Transistor Audio and Radio Circuits

The Mullard book "Transistor Audio and Radio Circuits" is intended as a manual of established and practical circuits for use by receiver and equipment manufacturers, radio and audio service engineers, university and college students, and do-it-yourself home constructors and hi-fi enthusiasts. A wide range of circuits is presented, extending from complete portable radio receivers to f.m. tuners and audio amplifiers capable of the highest standards of reception and reproduction. The audio amplifiers included in the book are listed below.

A. F. Amplifier Circuits

Output power (W, r.m.s.)	Total harmonic distortion (%)	Sensitivity (mV input for full output)	Recommended use
1	10	10	general purpose
3	1·7	70	general purpose
3	0·4 to 2	600	record player
4	1·2	0·4	tape recorder
5	2·5	43	car radio
6	1·2	52	car radio
10	2·9	80	general purpose
10	<0·1	430	high-quality systems
25	0·2	200	high-quality systems

Subjects include:

Pre-amplifiers for use with most a.f. circuits; r.f. circuits for a.m. and a.m./f.m. portable radios and car radios; auxiliary high-quality a.f. and r.f. "building block" circuits; high-quality f.m. tuners and stereo decoder; test equipment; hints on layout of high-quality a.f. equipment; biasing of r.f. circuits; useful charts and nomograms.

The book may be obtained from booksellers or Distributor Sales Division, Mullard Limited, Mullard House, Torrington Place, London, WC1E 7HD, price (U.K. only) 30/- plus 2/- postage.

Mullard Technical Handbook

Mullard data sheets are now available in new format: bound volumes have replaced the earlier ring binders which held loose data sheets. The Mullard Technical Handbook of data on components recommended for new equipment design now consists of fourteen such volumes which are grouped and labelled as parts of three main 'books'. Book 1 contains the data for semiconductor devices (including integrated circuits) and has six parts—or six volumes. Book 2 contains the data for valves and tubes and has five parts. Book 3 contains the data for passive components and materials and has three parts.

Each of the parts can be used on its own and consequently users need purchase only those parts which are relevant to their specific needs and interests. This can result in a considerable saving for most data users and can also save much valuable time if the data books are made correspondingly more easily accessible to individuals.

Three Ways In

Finding a wanted data page is made easy in the new format. First, a 'quick-reference thumb guide' is incorporated into the contents page and the page edges, so that sections can be located very rapidly. Second, there is an alpha-numerical index in each part, so that if the required type-number is known the wanted data can be found directly. Third, a well planned selection-guide is included in each volume, so that if the application for the component can be specified then all the likely component types and data pages are indicated immediately.

Updating

Updating of the data will occur annually, and new volumes should be purchased each year as required. About six months after each annual updating there will also be a much smaller supplement sent free for each part that has been purchased, and this will provide data for any new components within that part.

To obtain Mullard Technical Handbooks

The three data books (fourteen parts) are described individually below and can be ordered at a price of 12/– per part (post free) from Mullard Ltd., Mullard House, Torrington Place, London, WC1E 7HD. A descriptive brochure with an order form is available upon request.

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Part 5
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